ST. JOSEPH’S COLLEGE FOR WOMEN (AUTONOMOUS) VISAKHAPATNAM

III SEMESTER   **COMPUTER SCIENCE** TIME:3HRS/WEEK

CS-Ma3-3601(3) **COMPUTER ORGANIZATION** MARKS:100

w.e.f 2024-2025 (23AK Batch) **SYLLABUS**

**COURSE OBJECTIVES:**

To familiarize with organizational aspects of memory, processor and I/O..

**COURSE OUTCOMES:** Students after successful completion of the course will be able to:

1. Understand the basics of instructions [L2]
2. Evaluate the performance implications of hierarchical memory organization.[L3]
3. summarize various data transfer techniques.[L2]
4. Demonstrate an understanding of arithmetic operations and illustrate concepts of parallel processing.[L2]
5. Analyze the distinctions between microprogrammed and hard-wired control units.[L4]

**UNIT– I: Register Transfer Language and Micro Operations:** Introduction- Functional units, computer registers, register transfer language, register transfer, bus and memory transfers, arithmetic, logic and shift micro-operations, arithmetic logic shift unit.

**Basic Computer Organization and Design:** Instruction codes, instruction cycle. Register reference instructions, Memory – reference instructions, input – output and interrupt.

**UNIT–II: CPU and Micro Programmed Control:** Central Processing unit: Introduction, instruction formats, addressing modes. Control memory, address sequencing, design of control unit - hard wired control, micro programmed control.

**UNIT– III: Memory Organization:** Memory hierarchy, main memory, auxiliary memory, associative memory, cache Memory and mappings.

**UNIT – IV:** **Input-Output Organization:** Peripheral Devices, input-output interface, asynchronous data transfer, modes of transfer- programmed I/O, priority interrupt, direct memory access, Input – Output Processor (IOP).

**UNIT – V: Computer Arithmetic and Parallel Processing:** Data representation- fixed point, floating point, addition and subtraction, multiplication and division algorithms. Parallel Processing-Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline.

**Text Books:**

1. M. Moris Mano, “Computer Systems Architecture”, 3rd edition, Pearson/ PHI.

**Reference Books:**

1.Carl Hamacher, ZvonksVranesic, SafeaZaky, “Computer Organization”, 5th edition, McGraw Hill.

2. William Stallings, “Computer Organization and Architecture”, 8th edition, Pearson/PHI.

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**SUGGESTED CO-CURRICULAR ACTIVITIES & EVALUATION METHODS:**

**Unit 1:** Activity: Quiz competition on micro-operations.

Evaluation Method: Accuracy and speed in answering quiz questions.

**Unit 2:** Activity: Instruction Format Puzzle: Solving a puzzle to decode and understand instruction formats. Evaluation Method: Accuracy and speed in completing the puzzle.

**Unit 3:** Activity: Memory Hierarchy Poster: Creating informative posters or infographics on memory hierarchy. Evaluation Method: Clarity of information, presentation and creativity of visual design.

**Unit 4:** Activity: I/O Troubleshooting Challenge Evaluation Method: problem identification, feasibility of proposed solutions, and clarity of explanations.

**Unit 5:** Activity: Case Study on Parallel processing architecture. Evaluation Method: Understanding of parallel processing concepts and architectures.

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