ST. JOSEPH’S COLLEGE FOR WOMEN (AUTONOMOUS) VISAKHAPATNAM

II SEMESTER **COMPUTER SCIENCE** TIME:2Hrs/Week

CS-Ma2-2651(2) **DIGITAL LOGIC DESIGN** Marks:50

w.e.f. 2023-24 admitted batch (23AK) **PRACTICAL SYLLABUS**

1. Introduction to digital electronics lab- nomenclature of digital ICs, specifications, study of the data sheet, concept of Vcc and ground, verification of the truth tables of logic gates using TTL ICs.

2. Implementation of the given Boolean functions using logic gates in both SOP and POS forms

3. Realization of basic gates using universal gates.

4. Design and implementation of half and full adder circuits using logic gates.

5. Design and implementation of half and full subtractor circuits using logic gates.

6. Verification of stable tables of RS, JK, T and D flip-flops using NAND gates.

7. Verification of stable tables of RS, JK, T and D flip-flops using NOR gates.

8. Implementation and verification of Decoder and encoder using logic gates.

9. Implementation of 4X1 MUX and DeMUX using logic gates.

10. Implementation of 8X1 MUX using suitable lower order MUX.

11. Implementation of 7-segment decoder circuit.

12. Implementation of 4-bit parallel adder.

13. Design and verification of 4-bit synchronous counter.

14. Design and verification of 4-bit asynchronous counter.

**List of Experiments**

The laboratory work can be done by using physical gates and necessary equipment or simulators.

**Simulators:** https://sourceforge.net/projects/gatesim/ or https://circuitverse.org/ or any free open- source simulator.

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